Managing Power and Reliability of Integrated Systems

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UCSD
Introduction

- Systems on Chip (SOCs)
  - Designed as tightly interconnected set of cores
  - Deterministic design paradigm is increasingly harder to implement
    - parameter spread in deep submicron technologies, increasing system complexity, reduced noise immunity, power and thermal management issues

- Networks on Chips (NOCs, also known as Multi-Processor SOCs)
  - Treat SOCs as micro-networks in order to leverage uncertainty – assume incomplete knowledge of the environment
  - Interconnects designed using networking concepts
    - Multiple concurrent connections – higher bandwidth
    - Regular structure – optimized global wire design, modularity
    - Error correction/control – leverage ARQ, FEC etc. from networking
    - Traffic scheduling - lower latency
  - Big issue is a tradeoff between power, performance and reliability
    - Lower power consumption --> lower temperature, better reliability
    - But frequent switching between power states can cause a significant decrease in reliability – careful optimization is needed!
### Network on a Chip

![Network on a Chip Diagram]

### Specifications

<table>
<thead>
<tr>
<th></th>
<th>Audio</th>
<th>Video</th>
<th>Speech</th>
<th>Comm.</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active (mW)</td>
<td>700</td>
<td>1885</td>
<td>1500</td>
<td>1055</td>
<td>5140</td>
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<tr>
<td>Idle (mW)</td>
<td>216</td>
<td>235</td>
<td>1000</td>
<td>208</td>
<td>1659</td>
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<tr>
<td>Sleep (mW)</td>
<td>0.3</td>
<td>1.4</td>
<td>100</td>
<td>0.6</td>
<td>102.2</td>
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<tr>
<td>A-S-A (ms)</td>
<td>45.6</td>
<td>54.6</td>
<td>40</td>
<td>54.6</td>
<td>54.6</td>
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<tr>
<td>#DVS settings</td>
<td>11</td>
<td>11</td>
<td>3</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>DVS switch (us)</td>
<td>150</td>
<td>150</td>
<td>100</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

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Tajana Simunic Rosing
Power Manager Implementation

- Power management
  - Node-centric – fully contained in a local power manager
  - Network-centric – network power management requests
- Local power manager implements closed-loop power management:
  - Estimator
    - Observes incoming core traffic, core state & network PM requests
    - Estimates parameters used in recalculation of power management policy
  - Controller
    - Sets core’s energy and performance states based on estimator input
- Power management is based on Renewal Model

<table>
<thead>
<tr>
<th>Component</th>
<th>State</th>
<th>Distribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>User</td>
<td>Queue &gt; 0</td>
<td>Exponential</td>
</tr>
<tr>
<td></td>
<td>Queue = 0</td>
<td>Pareto</td>
</tr>
<tr>
<td>Device</td>
<td>Active</td>
<td>Exponential</td>
</tr>
<tr>
<td></td>
<td>Transition</td>
<td>Uniform</td>
</tr>
</tbody>
</table>

\[ \text{Exp} = 1 - e^{-\lambda e^t} \]
\[ \text{Pareto} = 1 - b \cdot t^{-a} \]
\[ \text{Uniform} = \begin{cases} \frac{t-t_{\text{min}}}{t_{\text{max}}-t_{\text{min}}} & t_{\text{min}} < t < t_{\text{max}} \\ 0 & \text{else} \end{cases} \]
Define:

- $T$: renewal time
- $T_a$: time of first request arrival
- $j_h$: time of transition to sleep from idle state

(j=index, h=time increment)

$$E[T] = E[T \mid T_a < j_h] + E[T \mid T_a > j_h]$$

- $E[\text{Length of idle period}]$ + $E[\text{Time service request}]$
- $E[\text{Length of idle period}]$ + $E[\text{Time to sleep}]$ + $E[\text{Length of sleep}]$ + $E[\text{Time to active}]$ + $E[\text{Time to service all requests}]$
Energy and performance are calculated for each state using:
- constant $C_i$ (e.g. power consumption in state $i$)
- expected time spent in the state, $E[T_i]$
- probability of the first request arrival, $P(T_a)$

<table>
<thead>
<tr>
<th>State</th>
<th>$C_i$</th>
<th>$E[T_{idle}]$</th>
<th>$E[T_{ToSleep}]$</th>
<th>$E[T_{Sleep}]$</th>
<th>$E[T_{ToActive}]$</th>
<th>$E[T_{SrvIdle}]$</th>
<th>$E[T_{SrvToSleep}]$</th>
<th>$E[T_{SrvToActive}]$</th>
<th>$E[T_{SrvSleep}]$</th>
<th>$P(T_a &lt; jh)$</th>
<th>$P(T_a ≥ jh)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>$C_{IS}$</td>
<td>$E[T_{ToSleep}]$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>$C_{S}$</td>
<td>$E[T_{Sleep}]$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Active</td>
<td>$C_{SA}$</td>
<td>$E[T_{ToActive}]$</td>
<td>$E[T_{SrvIdle}]$</td>
<td></td>
<td>$E[T_{SrvToSleep}]$</td>
<td>$E[T_{SrvToActive}]$</td>
<td>$E[T_{SrvSleep}]$</td>
<td>$P(T_a ≥ jh)$</td>
<td></td>
<td>$P(T_a &lt; jh)$</td>
<td>$P(T_a ≥ jh)$</td>
</tr>
</tbody>
</table>

$C_i = \{C_{IS}, C_{S}, C_{SA}, C_A\}$
Renewal Policy Optimization

- **Basic assumptions:**
  - general distribution governs the first request arrival
  - exponential distribution represents arrivals after the first arrival
  - user, device and queue are stationary

- **Optimize average performance under average power constraint**
  - randomized policy

\[
\begin{align*}
\min & \quad \sum_j d(j) p(j) \\
\text{s.t.} & \quad \sum_j T(j) p(j) = 0 \\
& \quad \sum_j p(j) = 1
\end{align*}
\]

Globally optimal policy calculated in seconds using LP
Formulate dual of the Lagrangian

\[ \text{Variables } v, u \text{ & } \lambda \text{ are the Lagrangian multipliers} \]

\[
\begin{align*}
\min & \quad v \\
\text{s.t.} & \quad d(j) + v(j)t(j) + u(j)[e(j) - t(j)P_{\text{constr}}] - \lambda(j) = 0 \quad \forall j
\end{align*}
\]

Obtain a minimum crossing point of a set of lines specified by the following equation:

\[
v(j) \leq \frac{d(j)}{t(j)} + u(j) \frac{[e(j) - t(j)P_{\text{constr}}]}{t(j)}
\]

Indexes of Lagrangian multipliers which form a solution, together with original constraints, are used to obtain the probabilities of transitioning into sleep state.

Real-time closed-loop control is possible

Globally optimal policy calculated in milliseconds
Node-centric estimation

- Estimation of exponential and Pareto distribution parameters

**Exponential**

\[ \text{Exp} = 1 - e^{-\lambda_e t} \]

- calculate maximum likelihood ratio for all rate settings
- calculate interarrival (or interservice) time sums (\( \sum t_j \))
- evaluate natural log of maximum likelihood ratio, \( \ln (P_{\text{max}}) \)

\[
\ln(P_{\text{max}}) = k \ln \frac{\lambda_{\text{new}}}{\lambda_{\text{old}}} - (\lambda_{\text{new}} - \lambda_{\text{old}}) \sum_{j=n_{\text{change}}}^{n_{\text{points}}} t_j
\]

- if ratio is larger than the one obtained from the lookup table, assume that the rate has changed

**Pareto**

\[ \text{Pareto} = 1 - b \cdot t^{-a} \]

- estimate parameters a & b using least-squares method on the log of Pareto distribution

![Graph showing probability distribution of idle time](image)
Controller implementation

- Consists of LFSR for generating probability & policy logic
- Controller on entry to idle state:
  - obtains a random number RND & finds \( j_h \) for which \( RND > p(j_h) \)
  - if no arrival during \( j_h \) seconds, the core enters sleep state, otherwise it stays active
- Frequency and voltage are set so the average expected processing delay in the queue is kept constant:
  \[
  Pr_{delay} = \frac{\lambda_{device}}{\lambda_{user} (\lambda_{user} - \lambda_{device})}
  \]

---

FPGA synthesis

<table>
<thead>
<tr>
<th>LFSR</th>
<th>LFSR Regs</th>
<th>Policy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits</td>
<td># LABs</td>
<td>Max ns</td>
</tr>
<tr>
<td>5-15</td>
<td>1</td>
<td>4</td>
</tr>
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</table>

---

Synposys synthesis

<table>
<thead>
<tr>
<th>LFSR Regs</th>
<th>Policy</th>
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<tbody>
<tr>
<td>#FFs</td>
<td>% area</td>
</tr>
<tr>
<td>5</td>
<td>14%</td>
</tr>
<tr>
<td>9</td>
<td>14%</td>
</tr>
<tr>
<td>15</td>
<td>12%</td>
</tr>
</tbody>
</table>
Network centric PM

Router

Core

Traffic

Network PM Request

Local Power Manager

Control Policy

Estimator

Core Function

Active State

foVo

queue > 0

Idle State

queue = 0

Transition to Active State

queue > 0

Transition to Sleep State

Network request

Renewal point

Arrival

Departure

Network request

No Arrival

Sleep State

Arrival

Transition to Sleep State

Network request

No Arrival

Arrival

queue = 0

Demand

Network request
Network centric PM implementation

- Estimator continues to have the same function as before
- Renewal model is expanded to include network requests
- Controller implementation changes:
  - When all network cores release the local core, the probability of transition to sleep is 1.0
  - As soon as a request comes from a network core to the local core, the local core transitions to the active state with probability 1.0
  - As soon as a request comes from a network core to the local core, the local core transitions to the active state with probability 1.0
- Node-centric PM is still needed to implement DVS and PM in situations when early network requests are not available

<table>
<thead>
<tr>
<th>Source</th>
<th>Idle Time (ms)</th>
<th>Transition Probability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Node</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>70</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>120</td>
<td>1</td>
</tr>
<tr>
<td>Network</td>
<td>Any time</td>
<td>1</td>
</tr>
</tbody>
</table>
Network-centric DPM increases power savings from a factor of 2.9 to 4.1, while at the same time reducing performance penalty by more than 10%.
Joint Power and Reliability Management
Integrated System Technology Issues

- Extremely small size
  - Thinner interconnect - more chance of EM failure
  - Thinner dielectric - more chance of TDDB failure
  - Narrower design margins
- Extremely large scale
  - High transistor density
    - Causes more failures
    - Enables redundancy
- Energy consumption
  - Increased energy consumption is a hurdle to modular redundancy
  - Power and thermal management are critical
    - Reliability exponentially related to temperature

Designing reliable integrated systems requires techniques that integrate with power management and tie to the underlying technology.
Hard errors

- Defects in silicon or package, permanent once present
- Integrated system lifetime is inversely proportional to the hard error rate
  - **Extrinsic**
    - caused by process and manufacturing defects
    - usually screened out before shipping a product
  - **Intrinsic**
    - occur during operation
    - depend on materials used, process parameters, system design and operating conditions
    - should occur after device passes its useful lifetime
    - Examples: electromigration, time dependent dielectric breakdown, thermal cycling
Electromigration (EM)

- Result of momentum transfer from electrons to the ions which make interconnect lattice
- Leads to opening of metal lines/contacts, shortening between adjacent metal lines, shortening between metal levels, increased resistance of metal lines/contacts or junction shortening
- Described by Black's model where $A_o$ is an empirically determined constant, $J$ is the current density in the interconnect, $J_{crit}$ is the threshold current density, $k$ is the Bolzmann's constant, $E_a$ and $n$ are 0.7 and 2

$$MTTF_{EM} = A_o (J - J_{crit})^{-n} e^{kT}$$

- Failure rate due to EM is modeled only in active and idle states as in sleep state leakage current is not yet large enough to cause migration:

$$\lambda_{core,s}^{EM} = A_o' (J_s - J_{crit})^n e^{-\frac{Ea}{kT_s}}$$

$\forall s = active, idle$
Time Dependent Dielectric Breakdown (TDDB)

- Wear out mechanism of dielectric due to electric field and temperature; causes formation of conductive paths through dielectrics shortening the anode and cathode.

- MTTF is a function of the empirically determined constant $A_0$, the field acceleration parameter $\gamma$, the electric field across the dielectric $E_{ox}$, the activation energy $E_a$, and temperature $T$.

\[
MTTF_{TDDB} = A_0 e^{\frac{E_a}{kT}}
\]

- Failure rate due to TDDB:

\[
\lambda_{core,s}^{TDDB} = A_0' e^{\gamma E_{ox,s}} e^{\frac{-E_a}{kT_s}}
\]

$\forall s = active, idle, sleep$
Temperature Cycling (TC)

- Caused by thermal cycles that occur during power state changes
  - Slow and fast thermal cycles
- Induces plastic deformations in materials - leads to cracks, short circuits and other failures of metal films and interlayer dielectrics
- Depends on temperature range and average temperature:

\[ N_f = C_o \left[ C_1 (T_{\text{max}} - T_{\text{min}}) - C_2 (T_{\text{avg}} - T_{\text{mold}}) \right]^{-q} \]

- Failure rate due to TC:

\[ \lambda_{\text{core,s}}^{\text{TC}} = C_o \left[ (T_{\text{active}} - T_s) - (T_{\text{avg,s}} - T_{\text{mold}}) \right]^{q} t^{-1} \quad \forall s = \text{sleep} \]
Basic Reliability Configurations

- **Active parallel configuration** has all redundant components working concurrently
  - Energy consumption is high
  - Time to transition on failure is very low
  - Failure rate is higher than standby parallel
  - E.g. identical controllers for a nuclear reactor

- **Standby parallel configuration** has redundant components in low-power mode until failure of the active component
  - Energy consumption lower
  - Time to transition on failure higher
  - Low failure rate
  - E.g. dual CPU platform

- **Series combination** has the highest failure rate
  - E.g. CPU, memory, interconnect

\[
\lambda_{fap} = \left(\sum_{i=1}^{M} (-1)^{i-1} \frac{C_i^M}{i\lambda_f}\right)^{-1}
\]

\[
\lambda_{sby} = \frac{\lambda_{fm}}{M}
\]

\[
\lambda_{core} = \sum_{i=1}^{N} \lambda_i
\]
Focus of this work

- Analyze system-level reliability
  - as a function of a power management policy
    - Analysis of single core and multiple core system
    - TC effect can dominate at small feature sizes, thus causing a large drop in reliability with aggressive power management policies

- Determine a system management policy
  - to maximize reliability and minimize energy consumption
  - Stochastic optimization problem
  - Time-indexed Markov chain model
    - Combined reliability with power management optimization
System analysis

- Analytical models are possible only under very strict assumptions on topology and failure rates
- Simulation of system evolution
  - For a given topology
  - For a given policy

- Challenges:
  - Stiffness of time constants
  - MTTF much longer than system transition times and environment arrival times of events
Simulator design

- Event-driven stochastic simulator
- Accepts any workload distribution, including raw data
- Input:
  - Reliability topology and failure mechanism characteristics (e.g. EM)
  - Power state specification
  - Workload
  - Time horizon
- Output:
  - MTTF, system reliability, energy consumption, performance
  - For a system of 10 cores runs in a few seconds
95nm technology
Video core becomes less reliable with lower temperatures as TC dominates; at higher temperatures EM and TDDB overpower TC so reliability improves
Audio core reliability falls with power consumption as TC mechanism dominates at all temperatures

<table>
<thead>
<tr>
<th></th>
<th>Pactive [W]</th>
<th>Pidle [W]</th>
<th>Psleep [W]</th>
<th>t_s [ms]</th>
<th>t_i [ms]</th>
<th>λtc [s⁻¹]</th>
<th>λworkload [s⁻¹]</th>
</tr>
</thead>
<tbody>
<tr>
<td>video</td>
<td>1.5</td>
<td>1</td>
<td>0.65</td>
<td>40</td>
<td>40</td>
<td>100</td>
<td>1</td>
</tr>
<tr>
<td>audio</td>
<td>0.7</td>
<td>0.2</td>
<td>3.00E-04</td>
<td>40</td>
<td>40</td>
<td>10</td>
<td>0.1</td>
</tr>
</tbody>
</table>
Markov processes model memoryless systems with constant failure rates
DPM&DRM - Power management modeling

- Environment
  - Active
  - Idle

- Queue
  - 4 3 2 1

- System
  - Active
  - Idle
  - Sleep
TISMDP Model for Joint DPM & DRM
(Time-Indexed Semi-Markov Decision Process Model)

- allows multiple decision states (e.g., multiple low-power states)
- more general and more complex method as compared to Renewal
- guarantees optimal results
- base model is Semi-Markov decision process model
  - applies to states with at least one exponential transition
- time-indexing is needed to account for time in states where more than one non-exponential transition occurs
- same basic assumptions as with Renewal model:
  - general distribution governs the first request arrival
  - exponential distribution represents arrivals after the first arrival
  - user, device and queue are stationary
**DPM&DRM System Model Details**

- **Combine:**
  - Power-state machine model - TISMDP
  - Reliability model - Markov process
- Represent overall system as combination of components’ PSMs where failure rates depend on system state
- System control aims to increase energy efficiency and enhance reliability
DPM&DRM Policy Optimization

Minimize average energy consumed under reliability and performance constraints – get randomized policy

\[
\begin{align*}
\min & \sum_{c=1}^{N} \text{cost}_{\text{energy}, c} \\
\text{s.t.} & \sum_{a \in A} f(s, a) - \sum_{a \in A} \sum_{s' \in S} M(s'| s, a)f(s', a) = 0; \forall s, \forall c_s \\
& \sum_{a \in A} \sum_{s \in S} T(s, a)f(s, a) = 1; \forall c_s \\
& \sum_{c=1}^{N} \text{cost}_{\text{perf}, c} < \text{Perf}_{\text{const}}; \forall c \\
& T_{\text{pl}}(\lambda_c) \leq \text{Rel}_{\text{const}}; \forall c_s \\
& \lambda_c = \sum_{i \in F} \sum_{a \in A} \sum_{s \in S} \lambda_{\text{core}}(s, a)y(s, a)f(s, a)
\end{align*}
\]

Variable definitions:
- \(\text{cost} (s,a)\): average cost incurred while in state \(s\) given action \(a\)
- \(f(\ s,a\ )\): frequency of executing action \(a\) while in state \(s\)
- \(M( s'| t, s, a)\): probability of arriving to state \(s'\) given action \(a\) taken in state \(s\)
- \(T( s, a)\): expected time spent in state \(s\) given action \(a\)
- \(T_{\text{pl}}(\lambda_c)\): reliability constraint as a function of network topology \(T_{\text{pl}}\)
- \(\lambda_c\): core reliability

Obtain globally optimal policy using linear programming

- Policy is obtained from state-action frequencies \(f(s,a)\) in form of a table of probabilities of issuing command \(a\) when system is in state \(s\)

\[
p(s,a) = \frac{f(s,a)}{\sum_{a' \neq a} f(s,a')}
\]
DPM Constraint Formulation

- **Energy and performance cost:**
  - $k(s_i, a_i)$ - lump sum cost
  - $c(s_{i+1}, s_i, a_i)$ - cost rate (e.g. power or performance penalty)
  - $F(t_i | s_i, a_i)$ - probability distribution of next event occurrence
  - $p(s_{i+1} | t_i, s_i, a_i)$ – probability of transition into next state $s_{i+1}$

$$\text{Cost}(s_i, a_i) = \begin{cases} 
  k(s_i, a_i) + \int_0^\infty \int \sum_{s_{i+1} \in S_{i+1}} F(du | s_i, a_i) c(s_{i+1}, s_i, a_i) p(s_{i+1} | t_i, s_i, a_i) dt \forall dt \\
  k(s_i, a_i) + \sum_{s_{i+1} \in S_{i+1}} c(s_{i+1}, s_i, a_i) T(s_i, a_i) \forall \Delta t
\end{cases}$$

- **Expected time spent in each state:**

$$T(s_i, a_i) = \begin{cases} 
  \int_0^\infty \sum_{s_{i+1} \in S_{i+1}} p(s_{i+1} | t_i, s_i, a_i) F(dt | s_i, a_i) \forall dt \\
  \int_{t_i}^{t_i + \Delta t} (1 - F(t)) \frac{dt}{1 - F(t_i)} \forall \Delta t
\end{cases}$$

- **Probability of arrival into each state:**

$$\text{M}(s_{i+1} | s_i, a_i) = \begin{cases} 
  \int_0^\infty p(s_{i+1} | t_i, s_i, a_i) F(dt | s_i, a_i) dt \\
  p(s_{i+1} | t_i, s_i, a_i) \Delta t
\end{cases}$$
Failure rate of each state is a sum of the failure rates due to all mechanisms (EM, TDDB, TC) acting in that state.

- Expected temperature in a state needs to be calculated:

\[
T_{state} = (T_{active} - T_{state,ss})e^{\frac{y(s,a)}{\tau}} + T_{state,ss}
\]

- Total failure rate of a core is a weighted sum of state failure rates, for example:
  - core has three power states: active, idle and sleep
  - two actions: “go to sleep” (S) and “continue” (C)

\[
\lambda_A y(A,C)f(A,C) + \\
\lambda_I y(I,C)f(I,C) + \lambda_I y(I,S)f(I,S) + \\
\lambda_S y(S,C)f(S,C) \leq \text{Rel}_{const}
\]

- System failure rate is calculated based on core topology as a function of series and parallel combinations.
Optimization Example: SOC Parameters

- 95nm technology
- Five cores; standard workloads (audio, video, www etc.)
- MTTF constraint set to 10 years; minimized power consumption

---

<table>
<thead>
<tr>
<th>IP block</th>
<th>$P_{\text{active}}$ [W]</th>
<th>$P_{\text{idle}}$ [W]</th>
<th>$P_{\text{sleep}}$ [W]</th>
<th>$t_{\text{ts}}$ [s]</th>
<th>$t_{\text{ta}}$ [s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP (TMS6211) [22]</td>
<td>1.1</td>
<td>0.5</td>
<td>0.01</td>
<td>250u</td>
<td>100n</td>
</tr>
<tr>
<td>Video (SAF7113H) [23]</td>
<td>0.44</td>
<td>N/A</td>
<td>0.07</td>
<td>110m</td>
<td>0.9</td>
</tr>
<tr>
<td>Audio (SST-Melody-DAA) [24]</td>
<td>0.11</td>
<td>0.03</td>
<td>3.00E-03</td>
<td>6u</td>
<td>0.13</td>
</tr>
<tr>
<td>I/O (MSP43011x2) [25]</td>
<td>1.00E-03</td>
<td>N/A</td>
<td>6.00E-06</td>
<td>100n</td>
<td>6u</td>
</tr>
<tr>
<td>DRAM (Rambus 512M) [26]</td>
<td>1.58</td>
<td>0.37</td>
<td>1.00E-02</td>
<td>16n</td>
<td>16n</td>
</tr>
</tbody>
</table>
Optimization Results – Single Core

- Maximum power savings achievable given MTTF of 10 years are at 90% for all cores and temperature ranges except for DSP, Video and Audio at 90°C due to TC mechanism.

- Design change effect - widening metal lines – plotted for each failure mechanism.

- Current density down by 20%, core area up by 5%, temperature down by 2%, but TC up by 10%.
Optimization Results - Redundancy

- Standby off and standby sleep redundancy model power savings with MTTF set to 10 years

- System meets MTTF of 10 years when one more redundant core in standby off mode is added to DSP, Audio and I/O; power savings of 40% are achieved
SOCs are rapidly evolving into NOCs
Reliability is of increasing concern and should be closely correlated with power management
This work presents an integrated methodology for analysis, optimization and management of reliability and power consumption:
- Simulator gives fast feedback on topology design and system characteristics for a wide range of operating conditions
- Optimizer provides a policy capable of giving an optimal implementation of reliability and power management control
Results obtained for a number of integrated systems implemented in 95nm technology show:
- Large dependence between power management policy and reliability due to tradeoff between EM, TDDB and TC effects
- 40% power savings on top of meeting MTTF of 10 years for an integrated system consisting of five cores with redundancy
SOC interconnect standards [AMBA, CoreConnect, VSI, OCP]

NOC architecture based on packet model
  - Fat tree router topology [Guerrier00]
  - Tiled architecture with flit-reservation flow control [Dally01]
  - Correct-by-construction protocol stack – MESCAL tools [Sgroi01]
  - Circuit and packet switched routing [PhilipsNOC03]

Reduction of energy consumption in NOCs (for overview see Benini04)
  - Maia processor has 21 satellite units; its configuration changes according to application needs – large energy savings [Wan00]
  - Energy efficient routing [e.g. Worm02, Yoshimura00, Nilsson03]
  - Node and network-centric power management suggested [Benini02]

Recently proposed power management systems
  - Exclusively node-centric, with little or no outside information utilized
  - Power management & dynamic voltage scaling occur separately
  - Open loop control
    - policies designed once with no further optimization at run time
Reliability - Related work

- Integrated simulation of power and reliability for processor design RAID [Bose et.al.’03]
- Fault-tolerant microarchitectures proposed in [Rotenberg’98]
- Redundancy at the architecture level [Shivakumar’03]
- Thermal management for multimedia [Srinivasan, Adve’03]
- Soft errors addressed by many, for example:
  - Ultra-low power systems [Maheshwari’02]
  - Sensing systems [Marculescu’03]
- Hard failure mechanisms studied at length in the past, e.g.:
  - Temperature cycling [Huang’00]
  - TDDB [Degraeve’98]