FPGA Design with Double-Gate Carbon Nanotube Transistors

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Outline

- Introduction
- Technology and Modeling of DG-CNTFETs
- Fine-Grain Reconfigurable Architecture
- Simulation Results
- Conclusions
Large Scale Directional Carbon Nanotubes

Large scale CNT technology

Asymmetrical Correlation of CNTs

Metallic-CNT-aware CNTFET technique

Fault tolerance of large scale CNTFETs

N. Patil et al., Sym. VLSI Tech. ’08

A. Lin et al., Sym. VLSI Tech. ’09
Ambipolar CNT Technology

- Ambipolar behavior reported on CNTFETs:
  - Conduction under both low and high gate voltage

- Technology demonstration with:
  - Undoped channel
  - Mid-gap D/S contact metal

- Polarity control with a double gate:
  - Double gate ambipolar CNTFET [Lin et al., TNANO’05]
  - P-type if low bias on back gate
  - N-type if high bias on back gate

- Ultimate goal:
  - Leveraging electrical benefits of CNTFETs: energy-delay-product (EDP) of CNTFET: 13x better vs. CMOS [Deng et al, ISSCC’07]
  - Controlling device operation (n- or p-type) during circuit operation
Demonstration of polarity tuning of double-gate carbon nanotube transistors (DG-CNTFET)

<table>
<thead>
<tr>
<th>$V_{fg}$</th>
<th>$V_{bg}$</th>
<th>state</th>
</tr>
</thead>
<tbody>
<tr>
<td>+V</td>
<td>+V</td>
<td>on (n)</td>
</tr>
<tr>
<td>-V</td>
<td>+V</td>
<td>off (n)</td>
</tr>
<tr>
<td>+V</td>
<td>-V</td>
<td>off (p)</td>
</tr>
<tr>
<td>-V</td>
<td>-V</td>
<td>on (p)</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>off (n/p)</td>
</tr>
</tbody>
</table>

Y.-M. Lin et al., TNANO '05

![Diagram of DG-CNTFET with current vs. $V_{gs-Al}$ graph showing p-branch and n-branch with different current levels and boundary for band-to-band tunnelling]
Fabrication of Ambipolar CNTFETs (2/2)

SOI substrate (only BOX and Si visible)
P++ doping of Si
Dry Si oxidation (top SiO₂)

CNT deposition or transfer

SiO₂
Si++

Dry Si oxidation (top SiO₂)

SiO₂
Si++

SiO₂

Si++

Al₂O₃ (or HfO₂) sputtering
Al sputtering (top gate)

Gate etch
Eventually SiO₂ etch (via opening)
Metallization (eventually different metals)
Double-Gate Channel Control

M. Najari et al, TED ’11
S. Frégonèse et al., TED ’11
Design of Static Ambipolar Logic Gates

\[
Y = \overline{A \oplus D + B \oplus E + C \oplus F}
\]

**GNAND-style structure**

\[
Y = \overline{(A \oplus D + B) \cdot C}
\]

**GAOI-style structure**

*De Marchi et al., Nanoarch ‘10*

*Ben Jamaa et al., DATE ‘09*
High Configurability of Ambipolar Logic Gates

<table>
<thead>
<tr>
<th>Ambipolar</th>
<th>Unipolar</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-input gates</td>
<td>4-input gates</td>
</tr>
<tr>
<td>15</td>
<td>GAOI4</td>
</tr>
<tr>
<td>10</td>
<td>GNAND4</td>
</tr>
<tr>
<td>6</td>
<td>AOI3</td>
</tr>
<tr>
<td>3</td>
<td>NAND3</td>
</tr>
<tr>
<td>4</td>
<td>NAND4</td>
</tr>
<tr>
<td>11</td>
<td>AOI4</td>
</tr>
</tbody>
</table>

Functionality of GAOI4

!A
A
!A + A·(!B)
(!A)·(!B)+A
(!A)·(!B)
A·(!B)
(!A)·(!B)+A·B
(!A)·(!C)+A·B·(!C)
(!A)·(!B)+(!A)·B·(!C)+A·(!B)
(!A)·(!B)+(!A)·B·(!C)+A·(!B)·(!C)+A·B
(!A)·(!B)·(!C)+A·B·(!C)
(!A)·(!B)·(!C)+(!A)·(!B)·(!C)·(!D)

Benchmark of functionalities
Reconfigurable FPGA Architecture

- CLB: complex logic block (logic macro-cell) with $I$ inputs and $N$ outputs
- CB: connection block (routing)
- SB: switch block (routing)
- BLE: basic logic element

Enhanced FPGA Architecture

Novelties:
- Replace memory-hungry LUT with ambipolar logic gates
- Include configuration information in data path
- Allow power signal polarity permutation
### Simulation Scenarios

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Logic type</th>
<th>N</th>
<th>I</th>
<th>Norm. CLB area</th>
<th>Intra-CLB delay (ps)</th>
<th>Inter-CLB delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>Reconf. ambipolar gates</td>
<td>1</td>
<td>4</td>
<td>2419</td>
<td>47</td>
<td>25</td>
</tr>
<tr>
<td>S2</td>
<td>LUT</td>
<td>1</td>
<td>4</td>
<td>2560</td>
<td>50</td>
<td>25</td>
</tr>
<tr>
<td>S3</td>
<td>Reconf. ambipolar gates</td>
<td>10</td>
<td>22</td>
<td>17167</td>
<td>200</td>
<td>423</td>
</tr>
</tbody>
</table>

- Fine-grain architectures have smaller area- and intra-CLB delay.
- They have a lower inter-CLB delay because of lower load on CLB in- and outputs.
- Gate-based architectures are more compact because of a lower need for memory and the compact gate design.
Synthesis Flow

- **Benchmark** → **ABC** → **Library builder** → **Logic Cell**
- **Genlib library**
- **Standard blif file** → **LUT-style blif file maker** → **LUT-style blif file**
- **Packing specs.** → **T-VPACK** → **net file**
- **Architecture file** → **VPR** → **Placement file**
- **Routing file**
Simulation Results

**Delay (ns)**

**Normalized area (million unit area)**

-13%  
-48%  
+10%  
-45%
Conclusions

- Double-gate carbon nanotubes FETs offer the opportunity to tune the device polarity.

- Reconfigurable FETs can be used in fine-grain reconfigurable logic circuits, such as FPGAs.

- These devices have a higher functionality that we leveraged in FPGAs design:
  - Compact logic, polarity permutation, configuration through the data path

- The approach offers faster FPGAs especially for fine-grain systems
Thank you for your attention

Questions?